International Journal of Application or Innovation in Engineering & Management (IJAIEM)
Web Site: www.ijaiem.org Email: editor@ijaiem.org, editorijaiem@gmail.com
Volume 2, Issue 7, July 2013 ISSN 2319 - 4847

High Performance CMOS Four Quadrant Analog Multiplier in 45 nm Technology

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Abstract

In this paper, a compact low-voltage CMOS analog multiplier is proposed. It is based on the square-law characteristics of the MOS transistor. The proposed circuit is obtained by rearranging circuit topology of a recently reported multiplier which is unpractical since the circuit topology itself needs an ideal voltage reference to form a multiplication function. By doing so, the ideal voltage reference is no longer required leading to achieve a new multiplier circuit with real compactness. Simulated results using TSPICE for 0.045µ CMOS process show that main performances of the proposed modulator including power consumption, noise, delay and bandwidth are successfully improved.

Keywords: CMOS, Analog Multiplier.

1. INTRODUCTION

Four-Quadrant analog multipliers are very useful building blocks in many circuits such as adaptive filters, frequency-shifters, and modulators. These applications are required to operate in low voltage environment for improving their power efficiency and incorporating with mixed signal systems to be used in portable applications [1]. According to [2], a four quadrant analog multiplier can be realized in many ways and it is also suggested by [3] that using saturated MOSFET in strong inversion is more practical than any other means. Recently, based on a square-law relation of saturated MOSFET, various compact multiplier architectures have been proposed [5]-[7].
In this paper, we report a four-quadrant analog multiplier circuit which is based on a similar technique [4] which has been realized in CMOS technology. This multiplier relies on the quadratic drain-current/ gate-voltage characteristics of MOS transistors operated in saturation. The proposed multiplier has been simulated in TSPICE by using model parameter for 0.045 µ CMOS process. The results show that power consumption, noise, delay of the proposed circuit is better than those of the circuit in [4].

2. BASIC CONCEPT

A CMOS four-quadrant multiplier can be used to multiply two bipolar signals, ±x and ±y. The multiplier circuit is a very useful building block and can be applied to any analog signal processing as well as analog filter, frequency doublers, modulator etc. Fig 1 [2] shows the basic block diagram of multiplying two inputs.

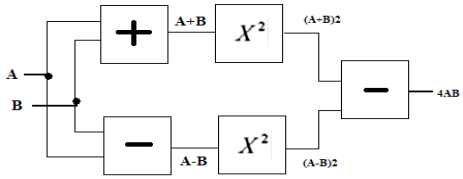

Figure 1 Block Diagram Of Multiplier Operation

The Quarter-Square Algebraic Identity as shown above is a famous method for an implementation of multiplier operation. There are 3 steps of this logic as described below:
1. Sum and Subtraction of both inputs A and B.
2. Take their results and square them.
3. Subtract the two squared output.
So the final output becomes:

$$V_0 = \left[(V_1 + V_2)^2 - (V_1 - V_2)^2\right] = 4V_1V_2 \qquad (1)$$

An excellent source of information on CMOS multipliers that operate in a multitude of modes such as saturation, triode, weak inversion, and others can be found. Here, operation in saturation seems to be preferable to the triode mode

because there are more options for multiplier topologies in saturation logic. A multiplier operation in saturation is possible only two transistors. This enables it to be used for low-voltage operations.

3. CIRCUIT DESCRIPTION SQUARE ROOTING CIRCUIT

3.1 Circuit Operation

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Another method is using a cross-coupled transistor pairs and floating voltage sources which also work in low-voltage. The circuit is based on the ideal *square-law* behavior of the MOS transistor in the saturation region, given by the expression

$$I_d = K(V_{GS} - V_t)^2 \quad (2)$$

with $K = 0.5.\mu_n.C_{ox}.W/L$, I_D the drain is current, V_{GS} is the gate-to-source voltage, V_T is the threshold voltage.

Realizing an analog multiplier and the multiplier in [7] is based on a similar approach showing in Fig. 1. It comprises a pair of common source amplifier (M1 and M2), which acts as input transistors to provide output currents in term of squaring functions of input voltages (*V*1 and *V*2), and two identical square root blocks. Injecting the output currents of the input transistors into the square root blocks, a differential output current of the overall circuit will become a multiplication function of two input signals *V*12 and *V*34.

Assuming the MOSFET M1 and M2 are biased in active region and neglecting channel length modulation effect, the current I_A and I_B can be respectively found as

$$I_A = K_n(V_1 - V_t)^2 \quad (3)$$

$$I_B = K_n(V_2 - V_t)^2 \quad (4)$$

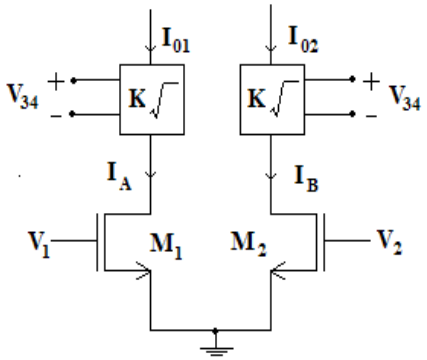

Figure 2 Realization of a four quadrant analog multiplier.

Where $K_n = 0.5.\mu_n.C_{ox}.W/L$ is a Trans conductance parameter of each MOSFET and V_t is the threshold voltage of NMOS transistor. From (3) and (4), the relationship between the current I_A and I_B and the differential input voltage $V_{12} = V_1 - V_2$ can be given by

$$\sqrt{I_A} - \sqrt{I_B} = V_{12}\sqrt{K_n} \quad (5)$$

The drain currents I_A and I_B are fed into the square root blocks controlled by V_{34}, results in

$$I_{out} = I_{01} - I_{02} = KV_{34}\left(\sqrt{I_A} - \sqrt{I_B}\right) \quad (6)$$

Where*K* is the gain of the square root blocks. Substituting (5) into (6), yields

$$I_{out} = K\sqrt{K_n}V_{34}V_{12} \quad (7)$$

It can be seen that an output current appeared in (7) is in form of a multiplication function between two input signals V_{12} and V_{34}. Based on this approach, both linear transconductor and four-quadrant analog multiplier have been proposed.

Unfortunately, the early works in [7] require more than 3V for supply voltage which is not sufficiently low for modern analog design. Subsequently, a new square rooting circuit operated under 1.5V single supply was proposed in [10] which can be applied as a compact four quadrant analog multiplier.

In the next section, the improved square root circuit which is more suitable for realizing an analog multiplier will be described.

3.2 Square Rooting Circuit

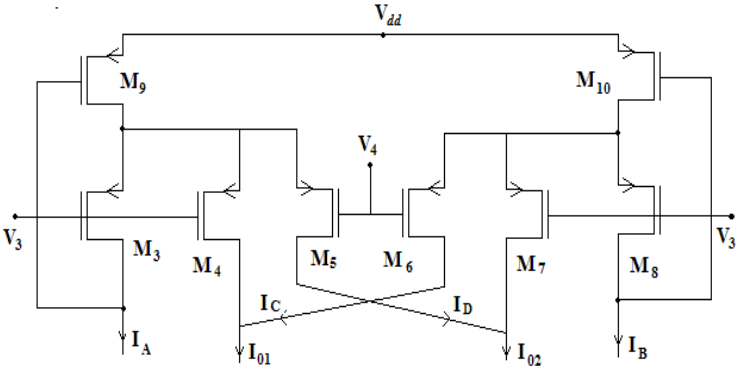

Figure 3 The square rooting circuit.

A square rooting circuit which is improved from Fig 2 is shown in Fig 3. Using square-law relation of saturated MOSFET in strong inversion and setting M3-M8 to be identical, the currents *Ic* and I_D are found to be

$$I_C = K_p\left(V_{34} + \sqrt{\frac{I_A}{K_B}}\right)^2 \quad (8)$$

$$I_D = K_p\left(V_{34} + \sqrt{\frac{I_B}{K_B}}\right)^2 \quad (9)$$

Where K_p is a transconductance parameter of each PMOS transistor and $V_{34} = V_3$-V_4 is a differential control voltage. Considering (6) and (7) in conjunction with the fact that I_A+ I_D= I_{o1} and I_B+ I_C= I_{o2} leading to

$$I_{01} = K_p V_{34}^{\ 2} + 2V_{34}\sqrt{K_p}\sqrt{I_A} + I_A + I_B \quad (10)$$

$$I_{02} = K_p V_{34}^{\ 2} + 2V_{34}\sqrt{K_p}\sqrt{I_B} + I_A + I_B \quad (11)$$

Subtracting (10) and (11), results in

$$I_{out} = I_{01} - I_{02} = 2\sqrt{K_p}V_{34}\left(\sqrt{I_A} - \sqrt{I_B}\right) \quad (12)$$

It is obvious that the output current of the improved square root circuit is a function of a square root of I_A and I_B and its gain can be adjusted by the voltage V_{34} and transconductance parameter K_p

3.3 Schematic Diagram of Four Quadrant Analog Multiplier using TSPICE

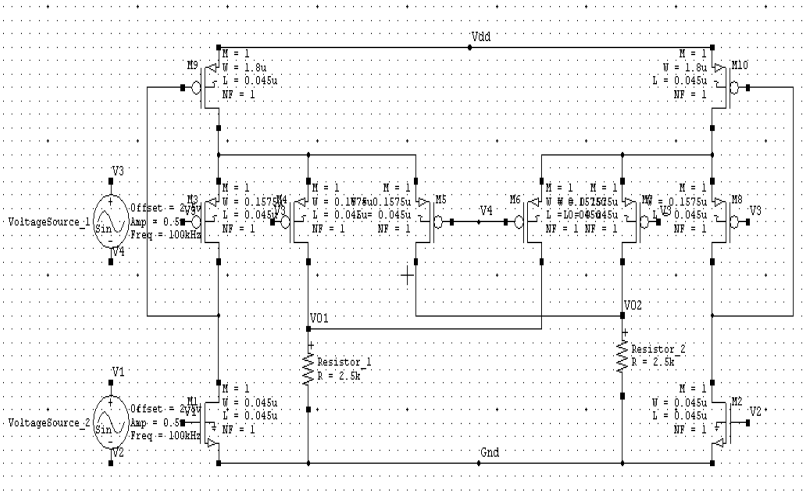

Figure 4 Schematic Diagram of Four Quadrant Analog Multiplier.

Fig.4.3 shows the proposed multiplier circuit which is constituted by substituting the square rooting circuit in Fig.4.2 into the square root blocks of Fig.4.1. Focusing on the differential output voltage we have found that

$$V_{out} = V_{01} - V_{02} = R\left(I_{01} - I_{02}\right) \quad (13)$$

Substituting (16) into (17), differential output voltage can be found as

$$V_{out} = 2RV_{34}\sqrt{K_p}\left(\sqrt{I_A} - \sqrt{I_B}\right) \quad (14)$$

Finally, substituting (5) into (14) yields

$$V_{out} = 2R\sqrt{K_pK_n}V_{34}V_{12} \quad (15)$$

Now, we have an output offset-free four quadrant analog multiplier and its gain can be adjusted by the load resistor R and the dimensions of each MOSFET.

4. SIMULATION RESULT

The multiplier circuit in Fig.4 is designed and simulated by using TSPICE for 45 nm CMOS process. The input voltage V_{12} and V_{34} are set to be balance with common mode voltages, respectively and supply voltage V_{DD} is set at 0.1V. Trying to avoid channel length modulation and short channel effects, the channel parameters of all transistors are set accordingly. Transistor parameters are listed in Table 1. The load resistors R are chosen to be 2.5 k. The power consumption, delay and noise have been listed in Table 2.

A 0.1V, 25 kHz sinusoidal carrier signal V_{12} shown in Fig.5(a) is multiplied by a 0.1V, 1 kHz sinusoidal modulating signal V_{34} shown in Fig. 5.(b). A resulting waveform is shown in Fig. 5.(c). Fig.6 shows simulated DC transfer characteristics of the proposed multiplier, when V_{12} was swept continuously from -0.3V to 0.1V while V_{34} was varied from -0.3V to 0.1V with0.1V step size. It can be observed that the linear range of $V_{12}$is approximately +0.4V.

Table.1: Transistor Parameters

Transistor	L(µm)	W(µm)	AS=AD(pm^2)	PS=PD(µm)
M1-M2	0.045	0.045	0.010125	0.54
M3-M8	0.045	0.1575	0.0354375	0.765
M9-M10	0.045	1.8	0.405	4.05

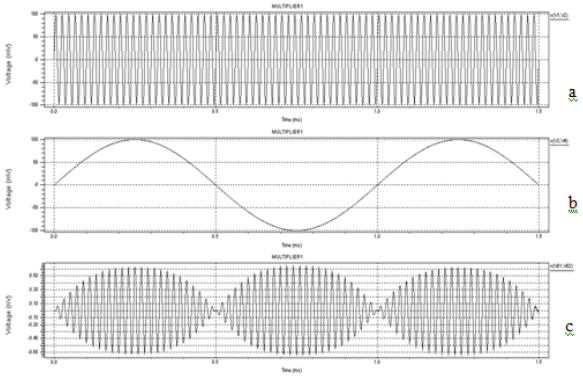

Figure 5 Schematic Diagram of Four Quadrant Analog Multiplier (a) V_{12} sinusoidal carrier signal (b) V_{34} sinusoidal modulating signal (c) Output waveform of amplitude modulator

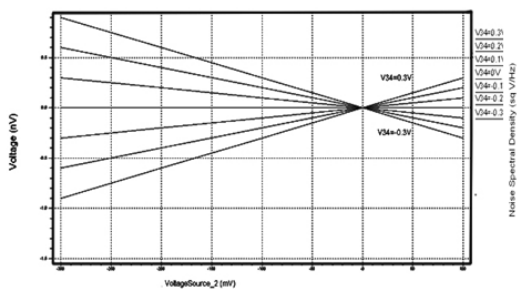

Figure 6 DC Transfer Characteristic

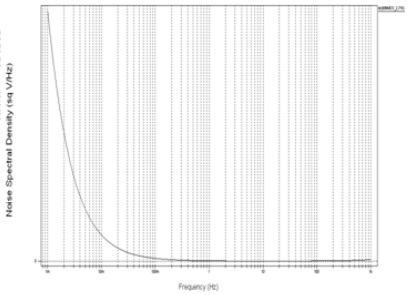

Figure 7 Flicker Noise Characteristic

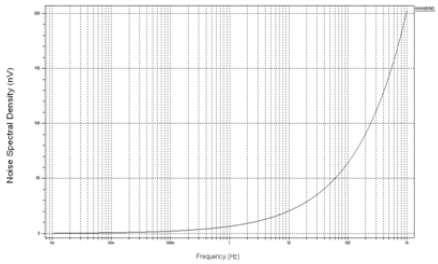

Figure 8 Total Output Noise Characteristic

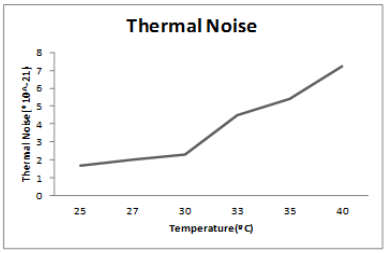

Figure 9 Thermal Noise Characteristic

Table.2: Output Data of Noise, Power and Delay in 45 nm Technology

Channel Length	Average Power Consumed (Watt)	Delay (Sec)	Flicker Noise (sq V/ Hz)	Thermal Noise (V)	Total Output Noise (V)
45 nm	6.006875×10^{-14}	5.3155×10^{-6}	5.3155×10^{-6}	5.3155×10^{-6}	5.3155×10^{-6}

5. Conclusion

A new square rooting circuit can be used for realizing a CMOS four-quadrant analog multiplier has been presented. The resulting multiplier circuit is improved to be more compact than the previous work. As a result, the proposed multiplier provides low noise, low delay and low static power consumption. Simulation results are given to verify the multiplier circuit performances.

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