

I-V Characteristic of CdO/PS Heterojunction

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Abstract

In this paper, CdO/porous Si heterojunction have been fabricated by high vacuum thermal evaporation of Cd on porous has been presented and annealing with temperature (300C). For the electrical properties of this structure have been studied and the optical properties of the CdO thin film are demonstrated. The electrochemical etching process has been used as a technique to control the porosity of silicon wafer by controlling the time of etching in the range (10,20,30,40) min. The results revealed that all our sample parameters are highly dependent on etching time. The minimum value of Filing Factor was (0.30) for the junction prepared by etching current density of (50mA/cm² for 40 min). The results of efficiency showed that these junctions had two depletion regions, the first one between CdO film and porous silicon layer, the second between the latter and the crystalline silicon. Minimum value efficiency was (1.61) for the junction prepared by etching current density of (50mA/cm² for 40 min). Maximum value efficiency was (9.71) for the junction prepared by etching current density of (50mA/cm² for 20 min).

Keywords: Porous Silicon, CdO thin films.

1. Introduction

In the last years, the researches regarding the physical properties of the transparent conducting oxides (TCO) in thin films are intensively stimulated due to their wide applications in the field of the electronic and photovoltaic devices. Among other (TCO) materials, cadmium oxide (CdO) continues to attract attention due to their interesting characteristics such as high electrical conductivity and optical transmittance in the visible spectral region. These properties make them very useful for applications in optoelectronic devices such as photodetectors, solar cells, gas sensors, antireflection coatings, etc. Many physical and chemical preparation techniques such as pulsed laser deposition, sputtering, spray pyrolysis, sol-gel, chemical vapor deposition, reactive evaporation, etc. have been used in order to obtain (CdO) coatings with required properties Other simple method used for preparation of different (TCO) thin films is the thermal oxidation of deposited metallic films Studies on the different metallic oxides in thin films obtained by this technique revealed that by the modification both of the deposition parameters for metallic films and the conditions of their post-deposition oxidation, the structural, electrical and optical properties of respective films can be influenced. However, until now, not much attention has been paid to the preparation of the (CdO) thin films by thermal oxidation of metallic Cd thin films^[1].(CdO) is regarded as a material with many attractive properties such large energy band gap, high transmission coefficient in visible spectral domain, remarkable luminescence characteristics etc. Bulk (CdO) is an n-type broad band gap (2.3 eV) semiconductor; with an indirect band gap of (1.36 eV) it has wide range of applications as solar cells, windows, flat panel display, photo transistors etc. It was experimentally established that structural, electrical and optical properties are very sensitive to the film structure and deposition conditions Such transparent conductors are being used extensively in thin film solar cells and optoelectronic devices (CdO)^[2] Transparent conducting oxides (TCO) constitute a unique class of materials which combine two physical properties together - high optical transparency and high electrical conductivity. These properties are generally considered to be mutually exclusive of each other since high conductivity is a property possessed by metals while insulators are optically transparent. This peculiar combination of physical properties is achieved by generating free electron or hole carriers in a material having a sufficiently large energy band gap (i.e., >_3.1 eV) so that it is non-absorbing or transparent to visible light. The charge carriers are usually generated by doping the insulator with suitable dopants and also by defects. It is no wonder that this unique material property makes (TCOs) technologically an important material and (TCOs) are widely used in commercial applications such as - in liquid crystal display (LCD), plasma and organic light emitting (OLED) displays; touch-screen sensors; thin film and organic photovoltaics, (OLED) lighting; low-e windows and smart windows; solar control film etc^[3].

2. Experimental Part

In this work, mirror-like p-type (boron doped) of (111) orientation mono-crystalline silicon wafers with electrical resistivity of (5) Ω.cm. Used First, the wafer scribed, cut into (1x1) cm² and cleaned carefully (to remove dirt and oil). Porous silicon was performed by electrochemical etching (anodization) using an electrolyte containing 40% HF acid with several drops of ethanol to prevent bubbling for different etching time (10, 20, 30 and 40 min) with a constant etching current density (50mA/cm²). Optical Properties for CdO film prepared on glass are calculated after measuring the transmittance of the film using a Double beam spectrophotometer provided by Shimadzu-Japan Company. (See Figure 1) electrochemical cell consists of the Si substrates set as anode and high purity PT wire set as cathode (forward bias) located

inside Teflon container filled with an electrolyte solution, power supply type was used to provide electric field. After etching the samples rinsed in water and ethanol, then do thin film was deposited on porous silicon and clean glass substrate by thermal evaporation technique as follows; high purity cadmium film (99.99%) provided from Aldrich Co. Was first deposited on Si using (Edward 216) coating system.

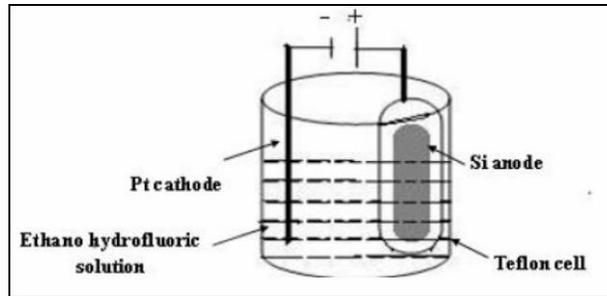


Figure 1 Schematic diagram of electrochemical anodization system [4]

CdO/PS, heterojunction, ohmic contacts are performed by evaporating of an Aluminum with a purity of 99.99%. The contacts are made on CdO/PS heterojunction by evaporating thin film (semitransparent) and thick of Al on front side (CdO) and backside (silicon), respectively. Spiral tungsten boat is used as a source of evaporation.

3. Results and Discussions

3.1 Optical properties:-

3.1.1 Transmission spectra of CdO film:-

Optical study of CdO film was carried out in the wavelength range (300–1100) NM at room temperature for the films deposited on glass substrate. Figure (2) shows that the transmission spectra of CdO films at different annealing temperatures (573, 673, 773 K) as a function of wavelength. The transmission is seen to increase after annealing due to the increase in crystallite size.

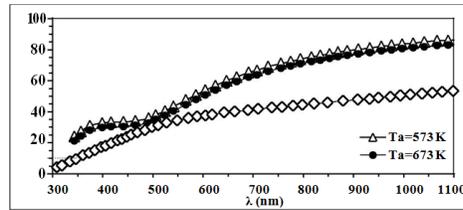


Figure 2 the transmittance spectrum of CdO thin films at different tea.

All the films are highly transparent in the visible region with an average transmittance of 81%. The sharp rise in transmission is an identification of good crystallinity of films. It is observed that the films obtained at higher annealing temperature shows slightly increase of transmittance in the visible region as compared to the films obtained at a lower annealing temperature. These results cause slight decrease in the optical band - gap of the film and it may be due to the increasing of grain size of prepared samples.

3.1.2 Absorption coefficient

The dependence of the absorption coefficient on the wavelength for different annealing temperatures (Ta) shown in figure (3).

In the shorter wavelengths, the absorption coefficient (α) exhibits high values which means that there is a large probability of the allowed direct transition, and then (α) decreases with increasing of wavelength.

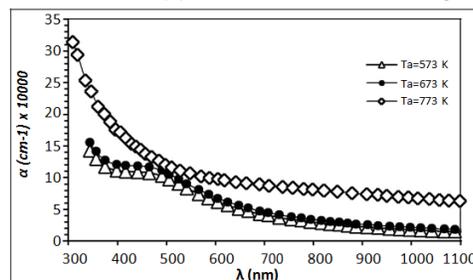


Figure 3 Absorption coefficients of CdO thin film at different tea

3.1.3 Optical band gap

The optical band gap E_g can be determined from transmittance data using Tauc relation [5] Where $(h\nu)$ is photon energy, (A) is a constant depending on the type of semiconductor, (n) is determined by the optical transition, and (α) is the absorption coefficient of the film can be calculated from transmission spectra by the relation (5) Where (d) is the thickness of the film. E_g is then determined by the extrapolation of the portion at $(\alpha = 0)$. The value of the optical energy gap decreases with increasing of T_a for all samples and this may be due to the increasing of grain size and the decrease in defect states near the bands and this in turn decreased the value of E_g [see table 1].

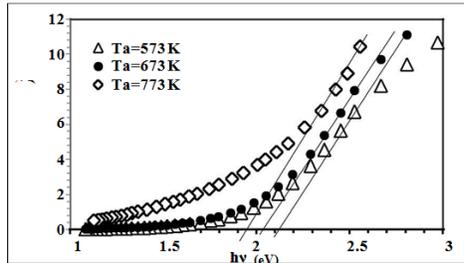


Figure 4 variation of $(\alpha h\nu)^2$ versus photon energy $(h\nu)$ for CdO thin film different T_a

Table 1 the energy band gap of CdO at different annealing temperature

Annealing temperature	Energy gap
573	2.3
673	2.04
773	1.95

3.1.4 Photoluminescence of CdO

The analysis of photoluminescence (PL) spectroscopy at room temperature reveals various peaks as shown in Figure (5). Using photoluminescence spectroscopy is to show the emission spectrum, since the most common radioactive transition in the semiconductor occurs between states at the bottom of the conduction band and the top of the valence band. The energy band gap can be determined from the photoluminescence spectrum of CdO film by using the following equation [6]:-

$$E_g = hc / \lambda$$

The room temperature photoluminescence spectra of CdO films at annealing (573, 673,773 K) is shown in Figure (5) at an excitation wavelength (340) nm . Three emission peaks are observed at 573K (625 nm), 673K (630 nm) and at 773K (630nm) for CdO thin film emission peak (Orange) refers to film in the region of the Visible. Red-shift from (1.98 to 1.96 eV) was caused by the formation of donor levels (Fermi levels) near the conduction band of the CdO.

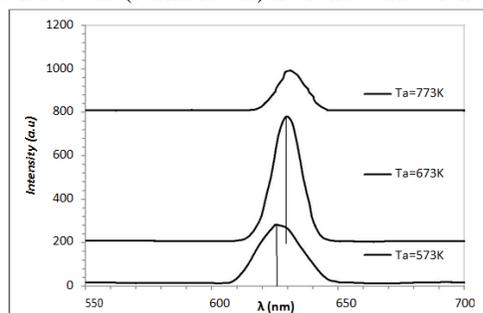


Figure (5) Emission spectrum of CdO at 340 nm excitation

3.2 Electrical properties for CdO/PS Heterojunction

3.2.1 I–V Characteristics of CdO/PS/P-Si Heterojunction

The Current-Voltage (I-V) characteristics of the fabricated device are illustrated at different etching time (10, 20, 30, 40 min). The dark (I_d) and photo illuminated currents are increased with increasing in the bias voltage. Figure (6) shows the (I-V) characteristics of (CdO/PS/P-Si) sandwich structure which contains (PS) layer prepared at the etching time (10, 20, 30 and 40 min), with a constant etching current density of $(50\text{mA}/\text{cm}^2)$ and $(5 \Omega \cdot \text{cm})$ p-type silicon substrate. The bias current contains two regions. In the first region of low voltage (<0.25) Volt, The current slightly increases with increasing of the applied voltage, and the generation current dominates, while at the second high voltage region (>0.25) Volt, the diffusion current dominates [7]. Also, the current–voltage characteristics exhibit rectification behavior may be due to the

hetrojunction potential barrier at the CdO/PS interface. The rectification factor indicates to the ratio between forward and reverse current at a certain applied bias voltage. The figure illustrates that the current flow in the forward bias decreases with increasing of etching time. Due to the high density of states of the PS layer which will result in screening of internal field inside the PS layer, This result explains the lowering of flow current in forward bias with increasing of etching time, since the porosity of PS layer increases with etching time and hence the resistance of PS layer becomes too high which leads to low forward current. The values of ideality factor are found to be (9.05) at etching time (10 min) about (8.94) at (20 min) etching time, (11.34) at (30 min) etching time and (14.12) at (40 min) etching time see table (3). That increase in ideality factor with increasing of etching time attributed to the increase in the density of states. These layer values of ideality factor demonstrate that the (PS) layer has a high density of states, so that there is no depletion region occurred at the (metal/ PS) interface and this contest should behave almost in an ohmic manner^[8]. Again, due to the high density of states of the PS layer which will result in screening of internal field inside the PS layer. In the reverse bias, also, there are two regions; one at low voltage, where the current increases with the applied voltage and the generating current is dominant. In the second region, the current is dependent on voltage and the diffusion current is dominant. When etching time increases the porous layer and the porosity increase, so that the pore walls act as carriers trapped and caused high resistivity which causes decrease in current^[9]

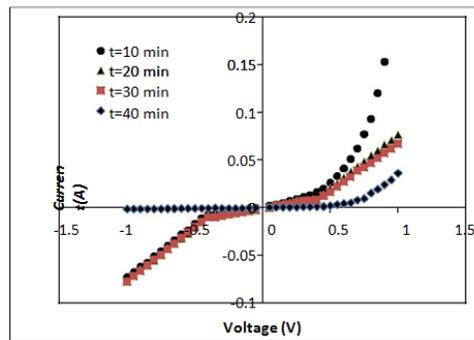


Figure 6 the I (V) characteristics of dark for CdO/ PS (HJ) at different etching time

Table 2 the variation of ideality factor and potential Barrier with etching time.

Etching Time (min)	Ideality Factor	Potential Barrier (eV)
10	9.05	0.564
20	8.94	0.57
30	11.34	0.587
40	14.12	0.608

The photocurrent is the current generated by the absorption of photons. It is considered as an important parameter, which acts on the spectral responsivity. Figure (7,8,9 and10) represents I–V characteristics under illumination with power intensities (35 mW/cm^2) at room temperature of the CdO/PS HJ. The photocurrent has been observed in reverse bias only, and we can see from this figure, that the presence of the light illumination strongly increases the reverse current. The photocurrent is always in the reverse bias direction because it increases by increasing the depletion region width. The increasing of the reverse bias voltage leads to the increase in the internal electric field which leads to an increasing in the probability of the separated electron – hole pairs. The photocurrent increases with increasing the incident power intensity, due to the increasing in the number of the generated photo carriers in the depletion region with the diffusion depth for carriers which depends on the life time of the minority carriers on the two sides of the depletion region^[10]. The effect of preparation conditions of PS layer such as etching time has very important effect on the photocurrent characteristics of the device, observe from figures (7,8,9 and 10) for etching times (10,20,30 and 40 min) respectively that the photocurrent is reduced with increasing of etching time. We can explain this result that the porosity of PS layer increases with increasing etching time. The increasing of porosity leads to increase the resistivity of PS layer; therefore, the photocurrent will decrease. The photocurrent is voltage dependent. At high reverse bias it saturates but for lower voltage, it tends to diminish. We think that, this behavior arises from the high resistance of the PS layer. When the resistance is small, the reverse current is just the sum of the saturation current and a voltage – independent photocurrent, however, high series resistance will limit the current at low voltage, and saturation will be observed only at high reverse bias. Under illumination the barrier collapses and the current will be limited by the resistance. Only for high reverse bias, the current will be so high that the barrier will control the behavior again.

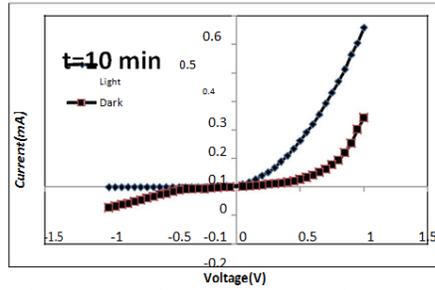


Figure 7 The I– V characteristics under illumination for CdO/PS (HJ) with etching time(10min) of PS layers

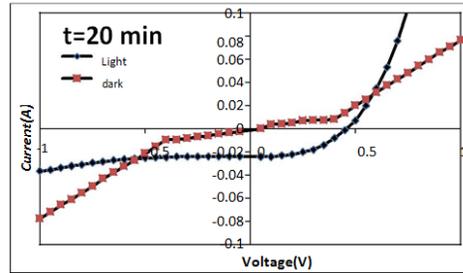


Figure 8 the I– V characteristics under illumination for CdO/PS (HJ) with etching time (20min)

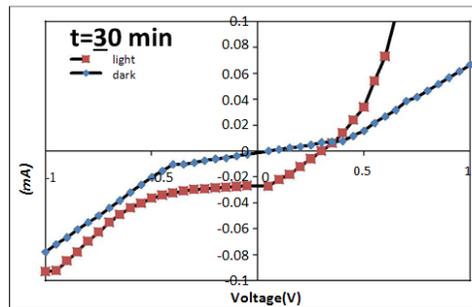


Figure 9 the I– V characteristics under illumination for CdO/PS (HJ) with etching time (30min)

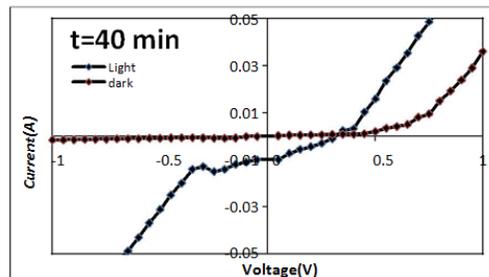


Figure 10 the I–V characteristics under illumination for CdO/PS (HJ) with etching time (40min)

The efficiency is a good parameter for (CdO/PS) because, it is represents the ratio between numbers of electron – hole generated in the (CdO/PS) due to the incident light and this parameter is a function of spectral responsivity. Table (3) Shows the variation of efficiency for (CdO/PS) prepared at different etching time (10, 20, 30 and 40 min) with constant current - density ($50\text{mA}/\text{cm}^2$), and it's found to be (9.71, 4.85, and 1.61) for different etching time (20, 30 and 40 min)respectively. The high efficiency at the time of etching 20min (9.71) . We showed that the photocurrent of PS prepared at etching time (20 min) is greater than the PS prepared at (40 min), because the decreasing of the porosity. Indeed, the increase in porosity leads to the increase of the electron-hole pairs number generated in the depleted region as a consequence of a decrease of absorbed photons by PS layer and of a strong absorption by silicon^[11]. The (V_{oc}) and (I_{sc}) increase where the fill factor decreases .The reason could be the lower fill factor caused by an increased series resistance. Also, it can explain the effect of enhanced voltage by ‘‘tandem effect’’ or multi-band gap cells. It should also consider the possibility that the optical absorption is simply enhanced due to light scattering in the porous Si, and formation of a

heterojunction between porous layer and Si substrate according to the quantum confinement model because of the larger band gap of PS layer compared to bulk silicon. The reduction of fill factor is a result of the lower electrical conductivity of the PS layer than silicon substrate which leads to a higher resistance of solar cells with PS layers^[12].

Table (3) parameters determined from I–V curves

Etching time (min)	I _{sc} (A)	V _{oc} (mV)	I _m	V _m (mV)	Efficiency	F.F
10	-----	-----	-----	-----	-----	-----
20	0.030	0.50	0.020	0.35	9.71	0.50
30	0.035	0.35	0.015	0.25	4.85	0.33
40	0.020	0.35	0.15	0.25	1.61	0.30

4. Conclusions

CdO/PS/P-Si heterojunction was successfully fabricated by using electrochemical etching of silicon and thermal evaporation of CdO. The optical and electrical properties of growing CdO are investigated. The electrical characteristics of heterojunction are strongly dependent on the etching current density and etching time. The junction parameters are estimated as a function of etching time. The process used here is simple, cheap, reliable and promising.

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