

Analytical Comparison of Predistorter circuits for DS-CDMA PA

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ABSTRACT

The design of a 3.0-7.0 GHz CMOS power amplifier (PA) for DS-CDMA application is presented. The Ultra Wide Band (UWB) PA proposed in this paper uses the cascade topology for common-source stage with a current-reused technique to achieve high power gain, and the analog predistorter linearization techniques to enhance the linearity of PA. The simulation results indicated a power gain of 37 ± 0.7 dBm for 4GHz bandwidth. The Power Added Efficiency (PAE) up to 25% over the frequencies ranges of interest. The output 1-dBm comparison is 15.4dBm at an input 1-dBm comparison is -19.5dBm.

Keywords: Power amplifier, Predistorter, Linearization techniques, DS-CDMA application

1. INTRODUCTION

The International Standard specifies the Ultra-wideband (UWB) system for a high-speed, and short-range wireless network, utilizing all or part of the spectrum of frequency bands from 3.1 to 10.6 GHz. This technology has attracted many researchers in both academia and industry to exploit this higher data rate and wider bandwidth wireless applications in comparison to others technology such as Bluetooth and WiMAX. This wireless technology is becoming more and more popular in many applications and the need to build compact, low cost and low power blocks arises [1].

To satisfy all the constraints UWB transceivers require the usage of wideband, low power and low cost circuits which further complicates design of RF front end blocks like power amplifier (PA) and low noise amplifier (LNA). Nowadays, the RF circuits are mostly realized in CMOS technology due to its advantages of low price, small size, high integration, and low power consumption [2].

The PA can drive the wanted signal without too many harmonic terms only in linear region operation. So, the linearity limits the actual power that can be driven to the load by the PA. One of the linearity merits is output 1-dB compression point (P1dB), which represents the nonlinear gain compression. Other major performance merits for a PA are power gain (PG) and power added efficiency (PAE).

In order to get maximum output power, the higher voltage swings at the output is needed. As compare with other topologies the common-source configuration has the large voltage swings [3]. In addition, the cascode configuration provides high isolation from the input to the output, and then improves the stability of the PA [4]. Class AB transistor can be used to achieve sufficient linearity and efficiency for delivering high output power [5]. However, the nonlinearity associated with Class AB amplifiers can seriously degrade the performance of the whole wireless system [6]. A Predistortion attempt to modify the signal's linearity before it is amplified, applying to the signal an inverse characteristic to the amplifier itself. Both the amplitude and phase characteristics of the PA should be compensated in the predistorter (PD). Radio Frequency (RF) Predistortion circuits are generally low cost, low power, easy to implement, and stable [7].

2. PREDISTORTION CIRCUITS

Simple analog PD mainly use a nonlinear resistive element such as a diode or a Field Effect Transistor (FET) channel as an RF voltage-dependent resistor, which can be configured to provide higher attenuation at low drive levels and lower attenuation at high drive levels [8].

2.1. Back-to-Back Diode

Fig. 1 shows two simple Back-to-Back Diode (BBD) pair shunted by a resistor inserted in series with the signal. As the input power increases, the series resistance of the diode decreases as its operating point is moved up the diode I-V curve. In shunt with the diode capacitance, its insertion loss becomes smaller and the phase decreases. When either circuit (a) or (b) is inserted prior to an amplifier with opposite characteristics, the cascaded AM-AM and AM-PM curves can be flattened and linearity improved over a range of input power levels, generally just below the 1-dB compression point of the amplifier [7].

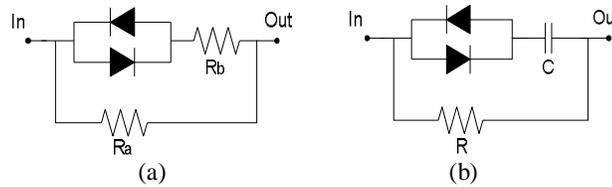


Figure 1 : Two typical diode predistorter circuits [7, 8]

2.2. Diode Connected MOSFET

The integrated diode linearizer in PA can effectively improve the gain compression and phase distortion performances by compensating the effects suffered from the gate dc bias level (V_{gs}) which decreases as the input power increases [9]. A CMOS implementation of this type of PD is based on the use of diode nonlinearities to provide the desired cancellation signal. A diode-connected MOSFET can be employed as shown in Fig. 2. In this figure, the square-law characteristic of the input signal is noted by observing that the source node of the MOSFET PD is at voltage V_{in} and that a dc bias voltage VDC is developed at the junction of the two resistors. The linear portion of V_{in} comes from the direct connection to the gate of the MOSFET PA. Extensive simulations must be performed to determine the bias voltage V_B for the MOSFET PD to ensure that the appropriate cancellation signal amplitude and phase are injected into the PA MOSFET [10].

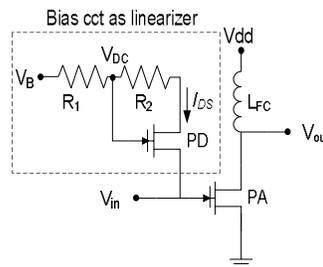


Figure 2 Diode connected MOSFET linearizer in PA [9]

2.3. Branch FET

The AC circuit diagram using a predistortion branch FET is shown in Fig. 3. A predistortion branch FET (FET2) is inserted in front of the main one so as to cancel out the inter-modulation distortion (IMD3) of the main FET (FET1). The method is based on the fact that IMD3 generated from main FET is nulled by that from a branch FET with optimized bias condition [11].

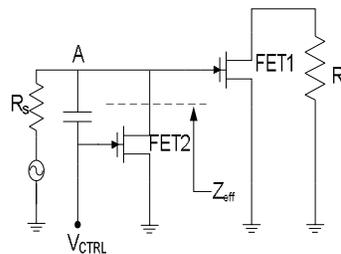


Figure 3 The AC circuit diagram of a Predistortion branch FET [11]

2.4. Anti-Parallel Diode Based Predistorter

The simplest form of third-order diode predistorter is shown in fig.4. The predistorter is formed around a T-attenuator (implemented by resistors R_1 - R_3) which serves to sample the main RF signal path and also to re-inject the distortion component back into that path. The nonlinearity itself is implemented by two anti-parallel diodes. If the diodes are perfectly matched then (ideally) only third-order distortion is generated and re-injected into the main path [12].

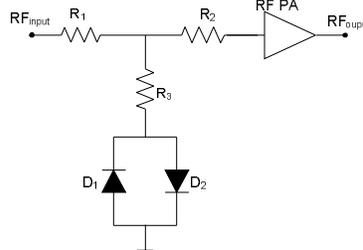


Figure 4 Anti-parallel diode based predistorter [12]

3. PROPOSED CIRCUIT DESIGN

The specifications of the DS-CDMA PA calculated based on the link budget of the entire transceiver, are given in Table 1. All the impedances of any RF block are terminated to 50 Ω, especially to aid in the testing of these blocks.

Table 1: DS-CDMA Specifications

Categories	Specifications
Power supply	1.8 V
Frequency range	3085.55~6934.8MHz
Output P1dBm	-2.0dBm
Input P1dBm	-17dBm
Power gain	15dBm
Gain flatness	± 1dBm

Fig. 5(a) shows a conventional cascode topology consists of a common-source (CS) M1 and a common-gate (CG) M2. This topology is often used for designing PAs due to many useful properties such as high output impedance. The gain is provided by the CS transistor M1 of the topology, M2 is mainly used to improve the reverse isolation. Therefore, the function of the CG stage of M2 should be revised to improve the gain. The cascode topology with current-reused is shown in Fig.5(b) consists of two CS amplifiers where M2 is also a CS amplifier converted from a CG amplifier by the current-reused. The current-reused function is implemented by Lg and Cg to boost the gain. The Lg has to perform series-resonance with Cg and the input capacitance Cgs2 of M2 to create a low impedance path to couple the output of M1 to the input of M2.

The series resonance circuit consists of Lg and Cg presents a narrow band characteristic. Therefore, the current reused function must be maximized at around the resonance frequency.

The proposed UWB PA for DS-CDMA application is divided into three stages: the PD circuit, a pre-amplifier and output amplifier as shown in Fig. 6. L2 and L4 are inductive peaking to achieve high gain at higher frequency. Capacitors C1, C3, and C5 are DC blocking, R1 and R2 are biasing resistors.

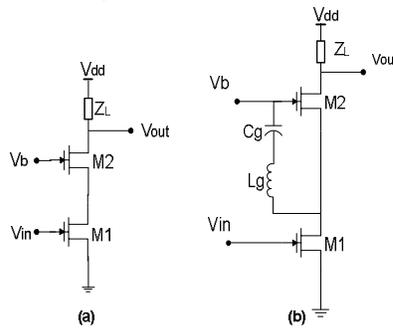


Figure 5 (a) Cascode amplifier, (b) Cascode topology with current-reused [1]

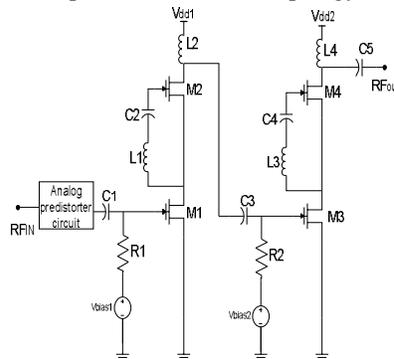


Figure 6 Proposed DS-CDMA PA circuit

4. RESULTS

The proposed 3-7GHz DS-CDMA with five PD circuits are simulated in MWO 2000. For comparison, the simulated results show the AM-AM and AM-PM for all five predistorter techniques BBD (a and b), diode connected MOSFET, Branch FET and Anti-parallel diode.

In order to test the linearity of the PA, the input signal power is swept from -25dBm to -15dBm, and the output power is plotted as a function of the input power. The linearity performances are evaluated by 1-dB compression point. The simulation results are shown in Fig. 7. The 1-dB compression output power is 15.4dBm at input power of -19.5dBm.

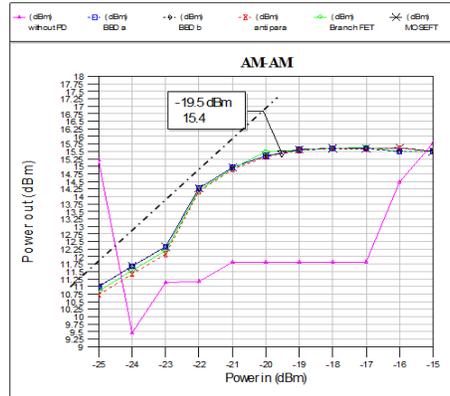


Figure 7 AM-AM measurement at 4GHz

An important specification for wideband communications is the Phase dispersion. Fig. 8 show the AM-PM for the PA without PD and all the predistorter circuits used. It is seen from Fig. 8, there is an increase in output power for the BBD(b) predistorter PA reach to 13dBm compared without PD. This improved output power is largely increase in branch FET circuit reach to 70.8dBm.

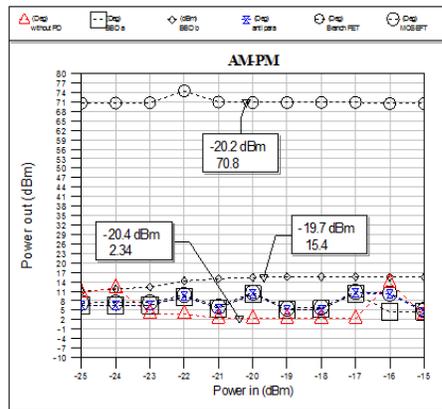


Figure 8 AM-PM measurement at 4GHz

Simulated PG of the proposed linear PA at -22dBm input power is shown in Fig. 9. The gain reaches to 37dBm for all PD circuits with a flatness of ± 0.7 dBm. The simulated PAE versus frequency 3-7GHz at -22dBm input power is shown in table 2. Branch FET is the best of all PD circuits used here as shown from all performance explained above.

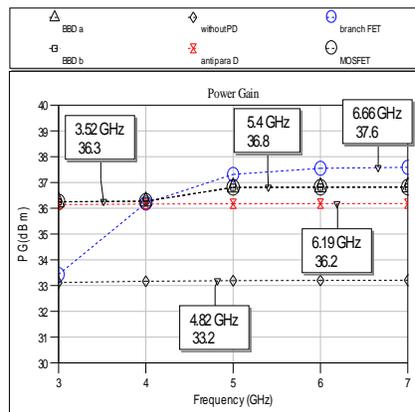


Figure 9 Gain Measurements at -22dBm input power

Table 2: Comparison of PD PAEs

PD circuits	PAE (%)
Back-to-back (a,b)	14-17
Anti-parallel diode	14
MOSFET	11-13
Branch FET	< 25

5. CONCLUSIONS

A 3 - 7 GHz CMOS PA using current reused and analog Predistortion linearization techniques is designed and simulated in the MWO 2000 package, for DS-CDMA application. The cascade with an additional CS stage topology is used to achieve high gain. The simulation results show that the PA achieves a gain of 37 ± 0.7 dBm with an output power of 15.4 dBm at an input 1-dB compression point -19.5 dBm. The proposed PA provides 4 GHz bandwidth, good flatness high gain, high linearity that can be implemented for UWB applications. This proposed design can be extended for uses up 3 - 10 GHz in the future due to the characteristic of current reused technique that can be used to enhance the gain at the upper end of the desired band.

REFERENCES

- [1] S.A.Z Murad, R.K Pokharel, H. Kanaya and K. Yoshida, " High Efficiency, Good Linearity, and Excellent Phase Linearity of 3.1-4.8 GHz CMOS UWB PA with a Current-Reused Technique ", Vol. 56, No. 3, IEEE, pp. 1241-1246, 2010.
- [2] J. Radic, M. Videnovic and V. G. Tavares "A Low-Power and High Gain CMOS UWB Power Amplifier for Group 1~3 MB-OFDM Application," Serbia, Belgrade, Nov. 23-25, IEEE, pp.783-786, 2010.
- [3] Y. Qian, W. Li and Z. Wang, "2.4-GHz 0.18- μ m CMOS Highly Linear Power Amplifier", IEEE, pp.210-212, 2010.
- [4] S. Ko & J. Lin, "A Linearized Cascode CMOS Power Amplifier", IEEE, 2006.
- [5] S.A.Z Murad, R.K Pokharel, H. Kanaya and K. Yoshida, " A 3.0-7.5 GHz CMOS UWB PA for Group 1~3 MB-OFDM Application Using Current-Reused and Shunt- Shunt Feedback", IEEE, 2009.
- [6] C. Wang, L. E. Larson, and P. M. Asbeck, " A Nonlinear Capacitance Cancellation Technique and its Application to a CMOS Class AB Power Amplifier", IEEE Radio Frequency Integrated Circuits Symposium, pp. 39-42, 2001.
- [7] R. Gilmore and L. Besser, " Practical RF Circuit Design for Modern Wireless Systems", Vol. II, Artech House Inc, 2003.
- [8] S. C. Cripps, "Advanced Techniques in RF Power Amplifier Design", Artech House Inc, 2002.
- [9] C. C. Yen and H. R. Chuang, "A 0.25- μ m 20-dBm 2.4-GHz CMOS Power Amplifier With an Integrated Diode Linearizer", IEEE Microwave and Wireless Components Letters, Vol. 13, No. 2, Feb. 2003.
- [10] R. Caverly, "CMOS RFIC Design Principles", Artech House Inc, 2007.
- [11] Kim, M., C. Kim, and H. Yu, "An FET-Level Linearization Method Using a Predistortion Branch FET", IEEE Microwave and Guided Wave Letters, Vol. 9, No. 6, pp. 233-235, 1999.
- [12] P. B. Kenington, "High-Linearity RF Amplifier Design", Artech House.

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