International Journal of Application or Innovation in Engineering & Management (IJAIEM)
Web Site: www.ijaiem.org Email: editor@ijaiem.org
Volume 3, Issue 4, April 2014 ISSN 2319 - 4847

Low Power 64bit Multiplier Design by Vedic Mathematics

Pranali Thakre[1], Dr. Sanjay Dorle[2], Prof. Vipin Bhure[3]

[1,2]Electronics & Communication Engineering, GHRAET, RTMN University, Nagpur, India
[2]Electronics Engineering GHRCE, Autonomous Institute, Nagpur, India

Abstract

ALU is the heart of any processor or the any complex system .To increase the speed of any system, it is required to increase the speed of ALU, but with low power consumption and for that portable life is required .VLSI designing techniques are the source to reengineering any digital electronics circuitry. In this paper a low power 64 bit ALU is designed using VERILOG .Low power consumption is achieved with Vedic multiplier and energy recovery adder .As multiplier and adder are the most important functioning part of ALU .The speed of ALU is mainly depend on functioning of adder and multiplier. The idea to design Low power ALU is adopted from Vedic Mathematics. for this purpose Urdhva Tiryakbhyam Sutra is used from Vedic mathematics, due to that the complexity of circuit will reduce and power also get reduced.

Keywords — Vedic mathematics ,Urdhva Tiryakbhyam Sutra ,Vedic multiplier

1. INTRODUCTION

Today ,'energy crises' is the main problem facing by the worldwide technologies. So, reducing the power consumption of any circuitry is the main task to overcome the energy crises problem. Ever increasing demand of technology required the processors to handle challenging and complex processes, results in to an assembling the number of processor cores on the single IC. But also the load on the processor not reduced in the generic system. For this purpose it have to implement main processor with co-processor to perform some specific operation like numeric computation, signal processing, Graphics etc.

Now a days, increasing demands of gadgets like laptops and tablets forcing the technology to develop the low power consuming and high speed processors. ALU is the heart of any processor. The speed of any processor is mainly depend on the computational time required to complete any task in the ALU. The speed of the ALU is mainly depend on its internal block functioning. Following fig.1 shows the basic blocks of the ALU. Amongst them the speed of ALU is mainly depends on the functioning of adder and multiplier. Adder and multiplier are the main fundamental blocks inside the ALU, on which its speed is depend. So implementing the high speed adder and multiplier to increase the speed of ALU is necessary.

Multiplier is the slowest element in the system. So optimizing it's area and increasing it's speed is the major designing task. This project work is deals with 'Designing of low power ALU by Vedic Mathematics'. Vedic Mathematics technique is used to implement first the Vedic multiplier of 64 bit to implement 64 bit ALU. For the calculation of multiplication Vedic sutra is used. An existing marginal algorithm or architecture can be designed by inserting new technology through a change at implementation level of design.

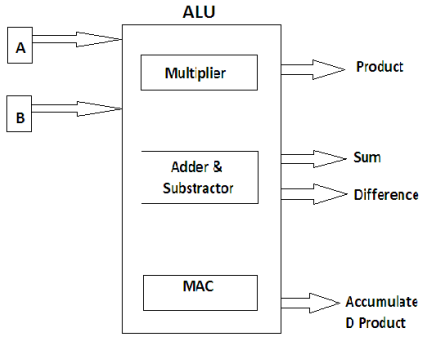


Fig.1 ALU Design

Vedic Mathematics

Vedic mathematics is the ancient system used for doing fast calculations in the mathematics. It is used in India from an ancient times. It is the gift for fast processing of mathematics calculations to this world from ancient stages. By using

Vedic mathematics for computation of algorithms of the coprocessor will reduce the computational time, complexity, power, area, etc. Vedic mathematics is based on the 16 sutras of Vedas, which are described below. This system is more simpler and faster than the modern mathematics. That's why we must be thankful to Jagadguru Swami Sri Bharati Krishna Tirthaji Maharaj who introduce Vedic mathematics and acknowledge the work of various people on Vedic mathematics. The 16 sutras of Vedic mathematics are described below with their meanings in alphabetical order.

1) (Anurupye) Shunyamanyat- If one is in ratio, the other is zero
2) Chalana-Kalanabyham-Differences and Similarities
3) Ekadhikina Purvena-By one more than previous
4) Ekanyunena Purvena-By one less than the previous
5) Gunakasamuchyah-The factors of the sum is equal to the sum of the factors
6) Gunitasamuchyah-The product of the sum is equal to the sum of product
7) Nikhilam Navatashcaramam Dashatah-All from 9 and the last from 10
8) Paraavartya Yojayet-Transpose and adjust
9) Puranapuranabyham-By the completion or noncompletion
10) Sanalana Vyavakalanabhyam-By addition and by substraction
11) Shesanyankena Charamena-The remainders by the last digit
12) Shunyam Saamyasamuccaye-When the sum is the same tha sum is zero
13) Sopaantyadvayamantyam-The ultimate and twice the penultimate
14) Urdhva-triyakbyham-Vertically and crosswise
15) Vyashtisamansthih-Part and whole
16) Yaavadunam-Whatever the extent of its deficiency.

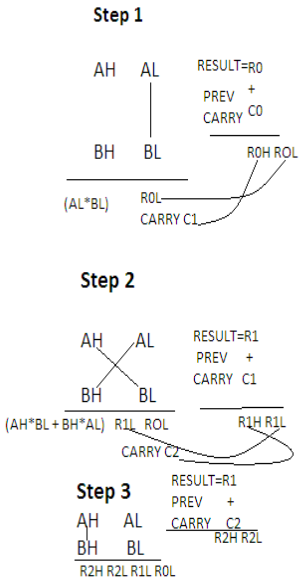
2. LITERATURE REVIEW

A. According to Anvesh Kumar, Ashish Raman, they gave the idea that Vedic sutras should be used to design the ALU. They suggest two sutras for the designing ofALU, Nikhilam Sutra,Urdhva triyakbyham Sutra. Multiply Accumulate block is extensibly used here. Multiplication algorithmis implemented using Verilog HDL. The multiplication algorithm is applying here only for 2 digit and 3 digit. The result is simulated using modelsim simulator.

B. According to V Jayaprakashan, V S Kanchana Bhaaskaran,this paper anlyses the use of an ancient mathematical approach for building an ALU. The arrangement of adders at architectural level is the main focus of this work. In this paper 4bit array multiplier is compared with 4bit Vedic multiplier and simulation is done in Spice Simulator.

I. Proposed Ttechnique

Urdhva Triyakbyham Sutra:



The sutras in Vedic mathematics helps to do almost all types of numeric calculations in easy and fast manner. This sutra is typically used for the multiplication purpose, applicable to all types of multiplication. Any bit binary number can be multiplied quickly by using this sutra. The meaning of this sutra is vertically and crosswise. Given below summarize the general process of the working of the Urdhva triykbyham sutra. For that we have consider here two number A and B having digits AH and AL for A number and BH and BL for number. The result is in the form R0,R1,R2 and each time

carry is added in to each product i.e.C0,C1,C2. So there will no carry propagation occur in the result due to which delay will be minimized.

By using this sutra the carry will not propogated up to the higher level,each time it will added to the product term,so time required to propogate carry up to higher level will be minimized. By designing this 2bit multiplier we have to design the 64 bit multiplier. Following block diagram shows the diagram for 64bit Vedic multiplier.in the following fig shows the block diagram,RTL view and technology schematic and output waveform of 64bit Vedic multiplier.

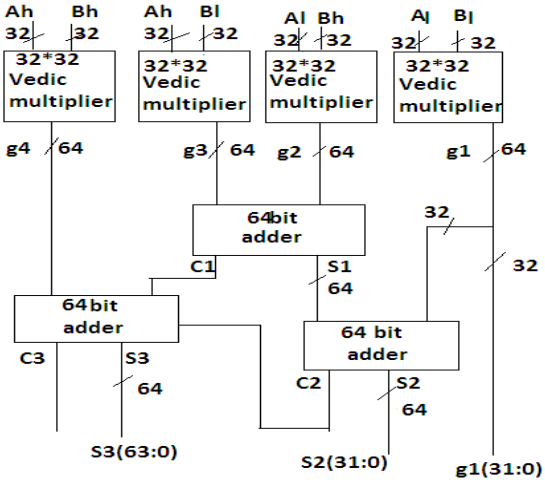


FIG.2 : BLOCK DIAGRAM OF 64BIT VEDIC MULTIPLIER

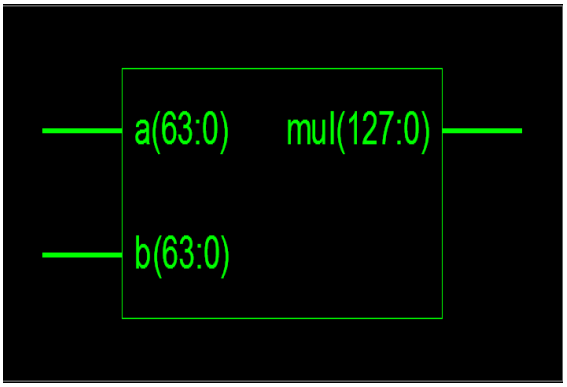


FIG.3 : RTL VIEW OF 64BIT VEDIC MULTIPLIER

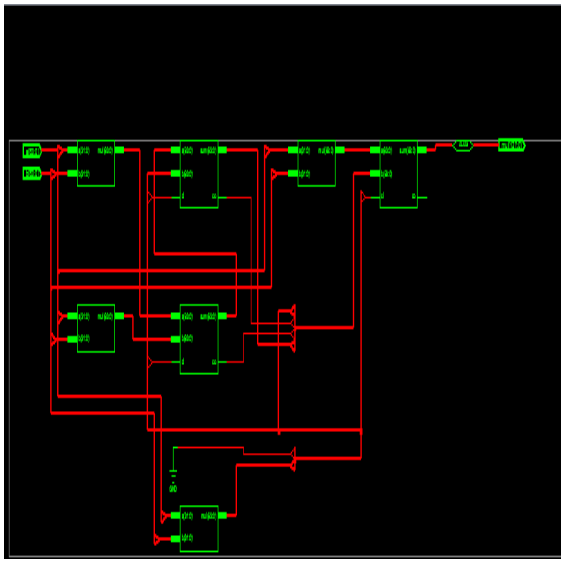


FIG.4 : SCHEMATIC REPRESENTATION OF 64BIT VEDIC MULTIPLIE

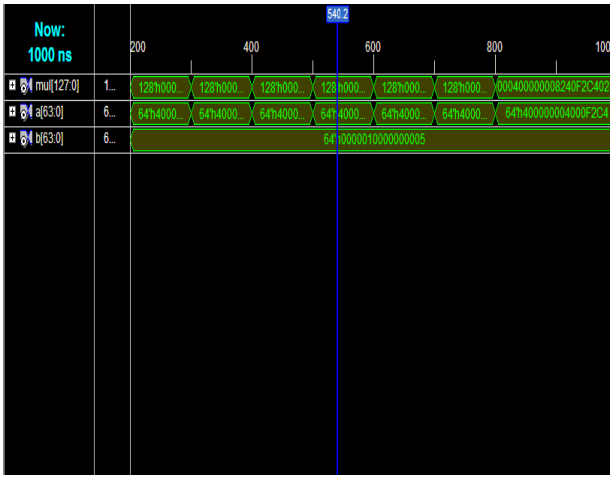


FIG.5 : OUTPUT WAVEFORM

3. Conclusions

The study in the paper shows the use of Vedic mathematics for designing the low power ALU. This paper presents the implementation of Vedic multiplier with the use of Urdhva triykbyham sutra,due to which carry will not propogated up to higher level, so propagation delay for higher number multiplication will reduce. So the speed of the multiplier will also increased. According to the above discussion it is most important issue to increase the speed and decrease the area of the multiplier,as it is the most important element in any of the processor or system. An implementation of Vedic mathematic techniques in designing of multiplier greatly improve the system performance and can be extended to reconfigurable architecture.

REFERENCES

[1] Anvesh kumar, Ashish raman, "Low Power ALU Design by Ancient Mathematics", 978-1-4244-5586-7/10, 2010 IEEE.

[2] V Jayaprakasan, S Vijayakumar, V S Kanchana Bhaaskaran,"Evaluation of the Conventional vs. Ancient Computation methodology for Energy Efficient Arithmetic Architecture",978-1-61284-764-1/11,2011 IEEE.

[3] Vaijyanath Kunchigi,Linganagouda Kulkarni,Subhash Kulkarni,32 Bit MAC Unit design usingusing vedic multiplier,ECC,JNTU,2013

[4] Kumar, A.; Raman, A.; "Low power ALU design by ancient mathematics", Computer and Automation Engineering (ICCAE),2010 The 2nd International Conference Publication Year: 2010 , Page(s): 862 – 865.

[5] Vaijyanath Kunchigi, Linganagouda Kulkarni, Subhash Kulkarni,"32-Bit Mac Unit Design Using Vedic Multiplier",International Journal of Scientific and Research Publications, Volume 3,Issue 2,February 2013.

[6] [6]Jagadguru Swami Sri Bharati Krisna Tirthaji Maharaja, "Vedic Mathematics Sixteen Simple Mathematical Formulae from the Veda,"1965.

[7] Sumita Vaidya and Deepak Dandekar, "Delay-Power Performance comparison of Multipliers in VLSI Circuit Design", International Journal of Computer Networks & Communications (IJCNC), Vol.2, No.4, pp 47-56, July 2010

AUTHOR

Pranali R. Thakre received BE degree in the year of 2012 in Electronics Engineering from Smt.Radhikatai Pandav College of Engineering.Now pursuing in M-Tech (VLSI)IInd year from Raisoni Acadomy of Engineering & Technology at MIDC Hingna.